MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table No.	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

PDS0101 – INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

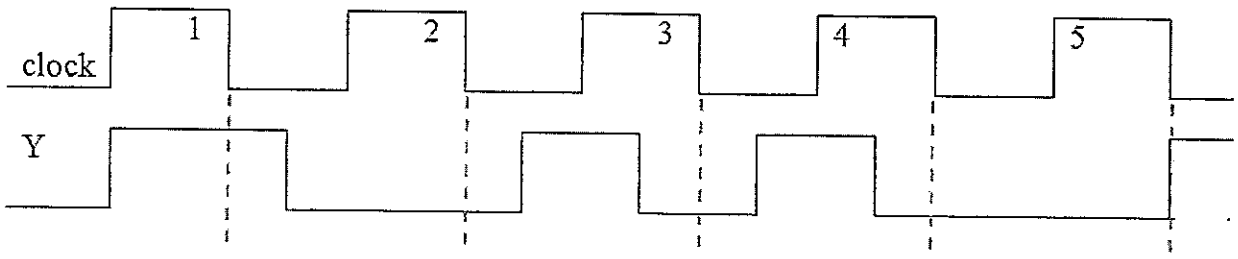
9 March 2018
3.00 pm - 5.00 pm
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of **9** pages including cover page with **5** questions. Please attempt **ALL** questions.
2. The total marks for this paper is **50** marks and the distribution of the marks for each question is given.
3. Please print all your answers in this booklet.

QUESTION 1

a) Referring to the square waveform Y shown in the image below, answer the questions that follow.



i. Determine whether the waveform is periodic or non-periodic. State your reason.
ii. Indicate the sequence of bits transferred if a bit is read upon the clock's falling edge.
iii. What is the time required to send one (1) bit if the given reference clock is running at 20 Hz?
iv. Calculate the total time required to send the bits you determined in (ii) for 2 bit parallel bus transfer.

[4 Marks]

b) Perform the following conversions from hexadecimal number to binary, octal and decimal numbers

	Binary	Octal	Decimal
$(78A)_H$			

[3 Marks]

Continued ...

c) Perform the calculation of $(33)_{10} - (29)_{10}$ using 8-bits signed 2's complement binary numbers and provide your answer in decimal. **[3 Marks]**

QUESTION 2

a) Identify the Standard Sum of Product form from the given Boolean expression

$$A\overline{C} + \overline{A}B + \overline{B}C$$

[3 Marks]

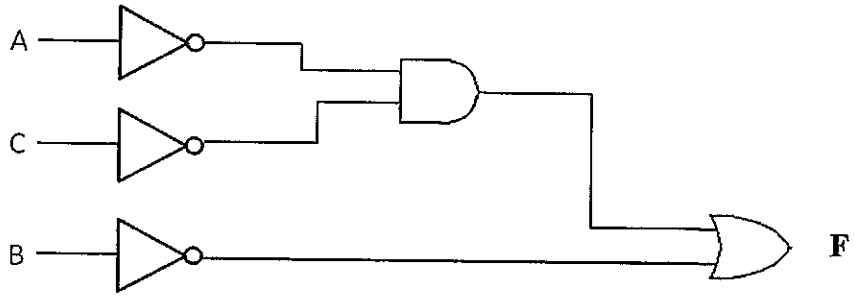
b) It is given that $K = \left(BC + \overline{A}\right)(A + \overline{B})$. Find the output of K by completing the truth table.

[4 Marks]

Continued ...

A	B	C	BC	$\overline{A}$	$BC+\overline{A}$	$\overline{B}$	$A+\overline{B}$	$K=\left(BC+\overline{A}\right)(A+\overline{B})$
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

c) Find the Boolean expression F from the circuit given below



[3 Marks]

Continued ...

QUESTION 3

a) Derive the Boolean expression of V in standard Sum of Products (SOP) format for the given truth table.

[3 Marks]

Input			Output
A	B	C	V
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

b) Apply K-map to minimize the above Boolean expression in SOP form and draw the simplified circuit.

[3 Marks]

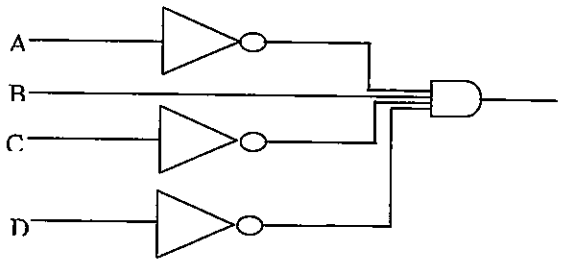
Continued ...

c) By applying Boolean rules and theorems, simplify the given expression P, and then draw the logic circuit for the simplified P. **[3+1 = 4 Marks]**

$$P = (AB + \overline{C})(D + \overline{AB}) + \overline{AD}$$

QUESTION 4

a) Determine the value (0 or 1) for each inputs (A,B, C and D) of this decoder, if the output is 1. **[2 Marks]**

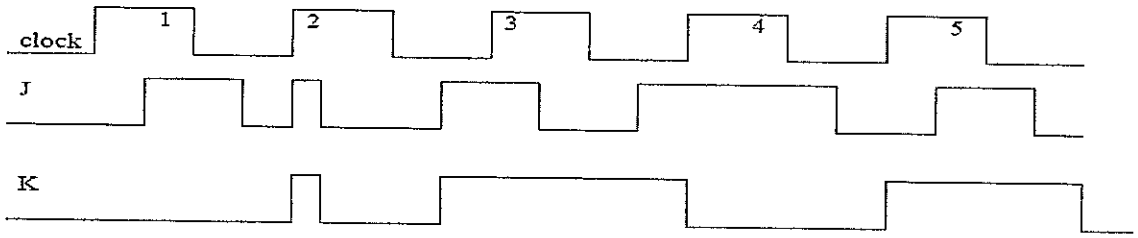


Continued ...

b) Design a 3-bit parallel adder by using three full adders, where carry output is represented by C_1, C_2, C_3, and sum of each bit adder is represented by $\sum_1$, $\sum_2$ and $\sum_3$. **[3 marks]**

c) By referring to the 3-bit parallel adder in (a), what is the result for C_1, C_2, C_3 and sum of each bit adder $\sum_1$, $\sum_2$, $\sum_3$ when 011_2 and 101_2 are added together. **[3 marks]**

d) For a negative edge triggered (NGT) J-K flip-flop with inputs as shown below, determine the Q (normal) output relative to the CLK assuming that Q is initially LOW. **[3 Marks]**



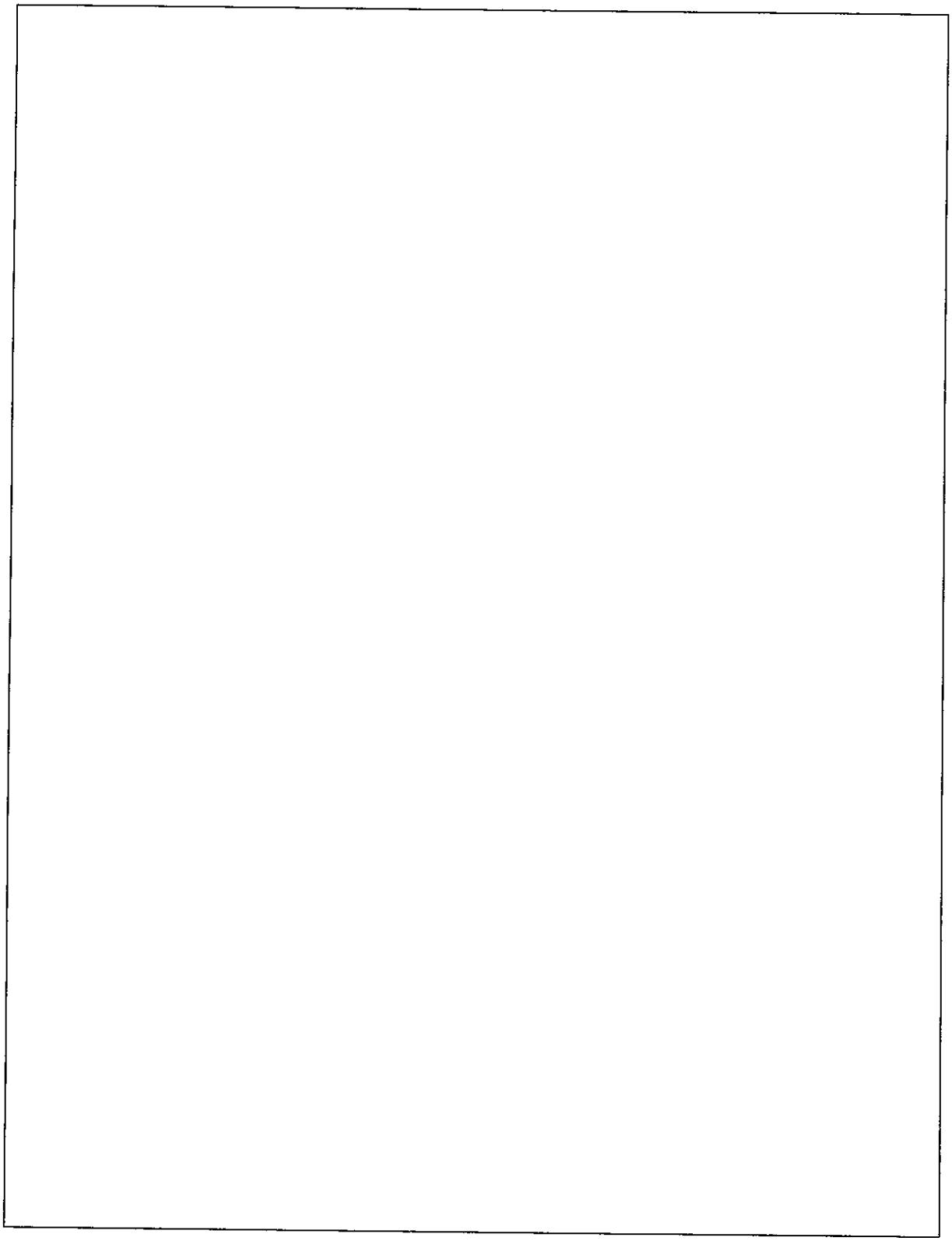
Continued ...

QUESTION 5

Design a synchronous counter using JK flip-flops that follows the sequence 001,011,101, 111 and repeats. The undesired states will go to do not care stage on the next clock pulse.

a) Construct the state diagram for the counter. **[2 Marks]**
b) Create the next state table according to the state diagram in (a) **[2 Marks]**
c) Use J-K excitation table to define the J and K inputs for each flip-flop involved in the counter. **[2 Marks]**
d) Perform K-map simplification for each of the flip-flops in the counter. **[2 Marks]**
e) Implement the simplified expressions as combinational logic using JK flip-flops to complete the design of the counter. **[2 Marks]**

Continued ...



End of Exam